WHAT IS CLAIMED IS:

1. A package for at least two semiconductor devices, the package comprising:

a first die including a first semiconductor device;

a second die including a second semiconductor device;

a DBC layer that includes a first metal layer, a second metal layer, and a ceramic material layer interposed between the first and second metal layers; and

a third metal layer to which the first metal layer of the DBC layer and the first die are attached,

wherein the second die is attached to the second metal layer of the DBC layer.

2. The package according to claim 1, wherein the second semiconductor device is a MOS device and the first semiconductor device is a bipolar device.

3. The package according to claim 2, wherein the bipolar device is a bipolar power transistor and the MOS device is a MOS power transistor, the bipolar transistor having a collector terminal directly electrically connected to the third metal layer.

4. The package according to claim 3, wherein the bipolar transistor is electrically coupled to the MOS transistor so as to form a cascode circuit.

5. The package according to claim 4, wherein the bipolar transistor has an emitter terminal electrically connected to a drain terminal of the MOS transistor.

6. The package according to claim 5, further comprising four pins, a first of the pins being electrically connected to a base terminal of the bipolar transistor, a second of the pins being electrically connected to the collector terminal of the bipolar transistor, a third of the pins being electrically connected to a source terminal of the MOS transistor, and a fourth of the pins being electrically connected to a gate terminal of the MOS transistor.

7. The package according to claim 6, further comprising a fifth pin for controlling a signal at the emitter terminal of the bipolar transistor.

8. The package according to claim 1, wherein the first semiconductor device is electrically coupled to the second semiconductor device.

9. An electronic system including a plurality of packages of semiconductor devices, at least one of the packages comprising:

a first die including a first semiconductor device;

a second die including a second semiconductor device;

a DBC layer that includes a first metal layer, a second metal layer, and a ceramic material layer interposed between the first and second metal layers; and

a third metal layer to which the first metal layer of the DBC layer and the first die are attached,

wherein the second die is attached to the second metal layer of the DBC layer.

10. The electronic system according to claim 9, wherein the second semiconductor device is a MOS device and the first semiconductor device is a bipolar device.

11. The electronic system according to claim 10, wherein the bipolar device is a bipolar power transistor and the MOS device is a MOS power transistor, the bipolar transistor having a collector terminal directly electrically connected to the third metal layer.

12. The electronic system according to claim 11, wherein the bipolar transistor has an emitter terminal electrically connected to a drain terminal of the MOS transistor.

13. The electronic system according to claim 12, wherein the at least one of the packages further comprises four pins, a first of the pins being electrically connected to a base terminal of the bipolar transistor, a second of the pins being electrically connected to the collector terminal of the bipolar transistor, a third of the pins being electrically connected to a source terminal of the MOS transistor, and a fourth of the pins being electrically connected to a gate terminal of the MOS transistor.

14. The electronic system according to claim 13, wherein the at least one of the packages further comprises a fifth pin for controlling a signal at the emitter terminal of the bipolar transistor.

15. The electronic system according to claim 9, wherein the first semiconductor device is electrically coupled to the second semiconductor device.

16. A method for packaging at least two semiconductor devices in one package, the method comprising the steps of:

providing a first metal layer;

attaching a first die, which includes a first semiconductor device, to the first metal layer;

attaching a DBC layer to the first metal layer, the DBC layer including a second metal layer, a third metal layer, and a ceramic material layer interposed between the second and third metal layers; and

attaching a second die, which includes a second semiconductor device, to the third metal layer of the DBC layer.

17. The method according to claim 16, wherein the second semiconductor device is a MOS transistor and the first semiconductor device is a bipolar transistor.

18. The method according to claim 17, wherein in the step of attaching the first die, a collector terminal of the bipolar transistor is directly electrically connected to the first metal layer.

19. The method according to claim 18, further comprising the step of electrically connecting an emitter terminal of the bipolar transistor to a drain terminal of the MOS transistor.

20. The method according to claim 19, further comprising the steps of:

electrically connecting a first pin to a base terminal of the bipolar transistor;

electrically connecting a second pin to the collector terminal of the bipolar transistor;

electrically connecting a third pin to a source terminal of the MOS transistor; and

electrically connecting a fourth pin to a gate terminal of the MOS transistor.

21. The method according to claim 16, wherein the first semiconductor device is electrically coupled to the second semiconductor device.